What is claimed is:

1. A method, comprising:

executing a first thread requiring a first valid virtual memory address representing a first physical memory address;

searching a translation look-aside buffer for the first valid virtual memory address;

retrieving a first translation upon failing to find the first valid virtual memory address;

searching the translation look-aside buffer for the first physical memory address; and

overwriting a second translation in the translation look-aside buffer corresponding to the first physical memory address with the first translation.

2. The method of claim 1, further comprising executing a second thread requiring a third translation corresponding to the first physical memory address.

3. The method of claim 2, wherein a multithreaded processor executes the first thread and the second thread.

4. The method of claim 3, wherein the multithreaded processor executes the first thread and the second thread using switch on event multithreaded processing.

5. The method of claim 3, wherein the multithreaded processor executes the first thread and the second thread using simultaneous multithreaded processing.

6. The method of claim 5 further comprising:

appending a first set of access rights for the first thread upon overwriting the second translation; and

appending a second set of access rights for the second thread upon overwriting the first translation.

7. The method of claim 6 further comprising:

erasing the first set of access rights if the third translation does not match the first translation.

8. The method of claim 7 wherein a content addressable memory is used to search the translation look-aside buffer.

9. The method of claim 1 further comprising:

creating a first one-hot index associated with the first physical memory address; and

validating the first valid virtual memory address using the first one-hot index.

10. A set of instructions residing in a storage medium, said set of instructions capable of being executed by a storage controller to implement a method for processing data, the method comprising:

executing a first thread requiring a first valid virtual memory address representing a first physical memory address;

searching a translation look-aside buffer for the first valid virtual memory address;

retrieving a first translation upon failing to find the first valid virtual memory address;

searching the translation look-aside buffer for the first physical memory address; and

overwriting a second translation in the translation look-aside buffer corresponding to the first physical memory address with the first translation.

11. The set of instructions of claim 10, further comprising executing a second thread requiring a third translation corresponding to the first physical memory address.

12. The set of instructions of claim 11, wherein a multithreaded processor executes the first thread and the second thread.

13. The set of instructions of claim 12, wherein the multithreaded processor executes the first thread and the second thread using switch on event multithreaded processing.

14. The set of instructions of claim 12, wherein the multithreaded processor executes the first thread and the second thread using simultaneous multithreaded processing.

15. The set of instructions of claim 14, further comprising:

appending a first set of access rights for the first thread upon overwriting the second translation; and

appending a second set of access rights for the second thread upon overwriting the first translation.

16. The set of instructions of claim 15, further comprising:

erasing the first set of access rights if the third translation does not match the first translation.

17. The set of instructions of claim 16, wherein a content addressable memory is used to search the translation look-aside buffer.

18. The set of instructions of claim 10, further comprising:

creating a first one-hot index associated with the first physical memory address; and

validating the first valid virtual memory address using the first one-hot index.

19. A processor, comprising:

a translation look-aside buffer to store a first translation corresponding to a first physical memory address;

a memory execution engine to execute a first thread to search the translation look-aside buffer for the first physical memory address and to overwrite the first translation with a second translation corresponding to the first physical memory address.

20. The processor of claim 19, wherein the memory execution engine executes a second thread requiring a third translation corresponding to the first physical memory address.

21. The processor of claim 20, wherein the memory execution engine executes the first thread and the second thread using switch on event multithreaded processing.

22. The processor of claim 20, wherein the memory execution engine executes the first thread and the second thread using simultaneous multithreaded processing.

23. The processor of claim 22, wherein the memory execution engine appends a first set of access rights for the first thread upon overwriting the first translation; and appends a second set of access rights for the second thread upon overwriting the second translation.

24. The processor of claim 23, wherein the multithreaded processor erases the first set of access rights if the third translation does not match the second translation.

25. The processor of claim 19, further comprising a content addressable memory to search the translation look-aside buffer.

26. The processor of claim 19, wherein the translation look-aside buffer contains a first one-hot index associated with the first physical memory address to validate the first valid virtual memory address.

27. A system, comprising:

a memory unit with data stored at a first physical memory address; and

a processor coupled to said memory unit and including a translation look-aside buffer to store a first translation corresponding to the first physical memory address; and a memory execution engine to execute a first thread to search the translation look-aside buffer for the first physical memory address and to overwrite the first translation with a second translation corresponding to the first physical memory address.

28. The system of claim 27, wherein the memory execution engine executes a second thread requiring a third translation corresponding to the first physical memory address.

29. The system of claim 28, wherein the memory execution engine executes the first thread and the second thread using switch on event multithreaded processing.

30. The system of claim 28, wherein the memory execution engine executes the first thread and the second thread using simultaneous multithreaded processing.

31. The system of claim 30, wherein the memory execution engine appends a first set of access rights for the first thread upon overwriting the first translation; and appends a second set of access right for the second thread overwriting the second translation.

32. The system of claim 31, wherein the multithreaded processor erases the first set of access rights if the third translation does not match the second translation.

33. The system of claim 27, further comprising a content addressable memory to search the translation look-aside buffer.

34. The system of claim 27, wherein the translation look-aside buffer contains a first one-hot index associated with the first physical memory address to validate the first valid virtual memory address.